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# ASYMMETRIC PARALLEL CONVERTER BASED HIGH-POWER STATCOM APPLIED TO BLDC MOTOR DRIVE

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## ABSTRACT

The recent power systems are typical networks where hundreds of power production stations and thousands of load centers are interlink through long power transmission and circulation systems. The primary enthusiasm of customers is the quality and dependability of power supplies at different load centers where they are put. Although the power generation in largest well developed countries is adequately trustworthy. The controller can adjust specific dc capacitor voltages when H-bridges run with unique exchanging examples and have parameter changes. This has couple of advantages: 1) the controller can work well in all operation modes and 2) the impact of the particular dc voltage controller on the voltage quality is limited. Diminished component number, easy layout for switches, and reduced dc-link capacitor values are the main features of the suggested topology over the diode clamped and cascaded multilevel converters. One of the control techniques of pwm phase-shifted carrier based pulse width modulation technique is implemented to rise the execution. The THD of the proposed concept can be carry out by adopting triggering pulses of distinct VSC's. The increased cost and complicated circuit model are the flaws of the design. An asymmetric parallel converter based high-power STATCOM is for power quality improvement. In this future scope output side BLDC drive is applied considering of this BLDC drive is much effective to correlate the other drives.

**KEYWORDS:** H-Bridge Inverter, Cascaded Inverters, Voltage Source Converter (VSC), Pulse Width Modulation (PWM), Static Compensator (STATCOM), Total Harmonic Distortion (THD), BLDC Drive

## INTRODUCTION

To give transmission-line voltage help, a static compensator (STATCOM) offers the ideal solution\ regarding value, unwavering quality, and element execution [2], [3]. For the most part, multipulse-converter-based [4] and multilevel converter- based [5]–[8] arrangements are utilized for high-control applications. A multipulse converter utilizes more than one voltage source converter (VSC), with basic dc connection, working with about principal exchanging recurrence, and the yield of every module is associated in arrangement through the multipulse transformer.

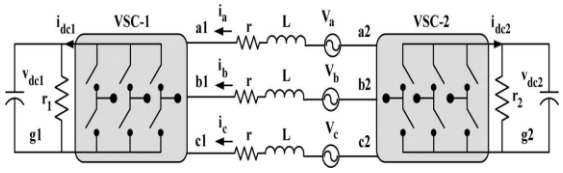


**Figure 1: Development of the Equivalent Circuit of the System**

Transformer is represented by equivalent series connection of inductances, resistances, and voltage sources. To model the losses in two VSCs, couple of resistances r1 and r2 is located side by side to the two dc links.

Multilevel converter innovation is an extremely effective option for medium-voltage and high-control applications furthermore for different applications where high voltages and currents are obliged [1], [2]. The other generally utilized multilevel topology, i.e, series converter topology [9]–[13], includes a few single-stage H-bridge/full-bridge converters, with particular dc links. The accompanying are the two related issues of this topology.

- The extent of the dc-link capacitor needed is high on the grounds that the prompt force included with every module fluctuates at double the essential frequency [14],
- Regulating voltage across a large number of self supported dc-link capacitors makes the controller design complex.

A power quality issue is characterized as any showed issue in voltage or current or prompting recurrence deviations that result in breakdown or mis-operation of client device. Power quality issues are connected with a broad number of electromagnetic aspects in power systems with wide scopes of time allotments, for example, long span varieties, brief time varieties and different unsettling influences. Brief time varieties are principally created by either blame condition or empowerment of expansive loads that oblige high beginning momentums.

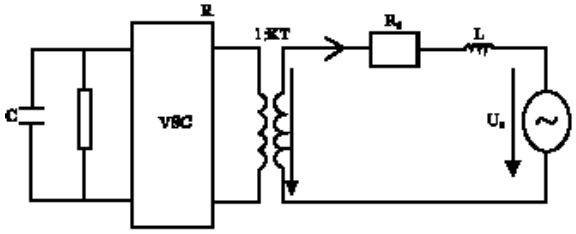


**Figure 2: Single-Phase Equivalent Circuit of STATCOM**

A single-phase equivalent circuit of STATCOM is shown in Figure 2. Where, $R_c$ is included to represent small losses in the switching devices of VSC. $R_s$ and L represent the equivalent circuit of the tie-transformer between system voltages $U_s$ and the output voltage $U_I$ of STATCOM.

Therefore, standard VSC power modules [include six insulated-gate bipolar transistors (IGBTs) and their driver circuits in one package] can be used instead of discrete components. Moreover, this topology utilizes cascade connection of three-phase VSCs, and hence, the size of the dc-link capacitor is less as compared to that in cascaded H-bridge multilevel converter. Most power-electronics technologies, including control skills, are required to convert the dc into ac power. The open-ended transformer topology has similar component layout with twin converter topology, reported in [2]. In the twin converter topology, the dc-link voltages of both VSCs are maintained equal. Therefore [9], only three-level operation is achieved. However, in the open-ended transformer topology, the dc-link voltage of VSC-2 is regulated to half that of VSC-1. This ensures four-level operation of the circuit [1]. Therefore, low THD is achieved with reduced filter requirements as compared [3] to three-level twin converter topology. The diode-clamped inverter uses a single dc bus that is subdivided into a number of voltage levels by a series string of capacitors [1]. A matrix of semiconductor switches and diodes allows each phase-leg output to be switched to any of these voltage levels.

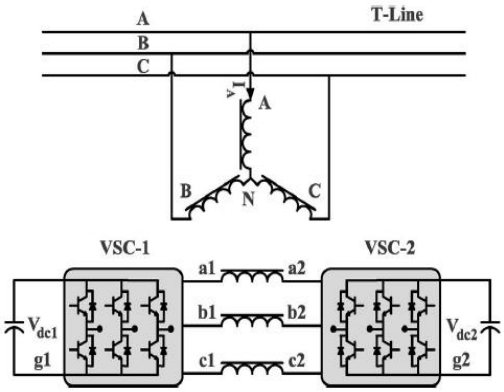


**Figure 3: Asymmetric-Twin-Converter-Topology-Based STATCOM**

To address this limit, an asymmetric twin converter topology is proposed in this paper wherein just two dc connections are utilized without spilt capacitor arrangement, as indicated in Figure 3. Moreover, the THD of currents supplied to the network is decreased by selecting a suitable degree of dc-link voltages of the two Vscs.

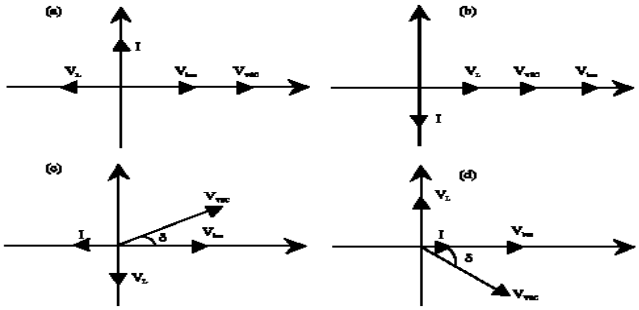

**Figure 4: Vector Diagram of STATCOM (a) Capacitive Mode, (b) Inductive Mode, (c) Active Power Release and (d) Active Power Absorption**

## MULTILEVEL CIRCUIT TOPOLOGY

- **Principle of Operation**

By changing the triggering pulses of distinctive Vscs, defined (THD) of the injected current is attained to with lessened switching losses as contrasted with that of single-VSC-based arrangement. The significant disadvantage of this plan is the high cost and complex structure of the massive multipulse transformer. To address a portion of the previously stated confinements in multilevel converters, a four-level open-ended transformer-based multilevel converter, is proposed in [1].

The proposed asymmetric twin-converter-based multilevel topology, having two Vscs, is indicated in Figure 3. Low voltage (LV) windings of the transformer are associated differentially between two 2-level Vscs such that the voltage showing up on the LV side is the distinction of the yield voltages of two Vscs. High-voltage (HV) windings, located in a star arrangement, are joined with the three-stage grid. Leakage inductances of the transformers go about as input filter inductances of the STATCOM. Both Vscs work with independent dc links to create two-level individual yield. Voltages showing up on the LV windings of the transformer are composed regarding yield voltages of Vscs as

$$e_a = e_{a1g1} - e_{a2g2} + e_{g1g2}$$
$$e_b = e_{b1g1} - e_{b2g2} + e_{g1g2}$$
$$e_c = e_{c1g1} - e_{c2g2} + e_{g1g2} \quad (1)$$

Where $e_a$, $e_{a1g1}$, $e_{a2g2}$, and $e_{g1g2}$ are the voltages across the LV winding of phase-a, the pole voltage of VSC-1, the pole voltage of VSC-2, and the voltage difference between negative dc-link terminals of the two VSCs, respectively. Since both VSCs have separate dc links, the sum of the LV winding phase currents should be zero

$$i_a + i_b + i_c = 0. \quad (2)$$

Furthermore, the sum of instantaneous values of grid voltages is equal to zero

$$v_A + v_B + v_C = 0. \quad (3)$$

The sum of the LV winding voltages is given by

$$e_a + e_b + e_c = \frac{N_{\mathrm{LV}}}{N_{\mathrm{HV}}}(v_A + v_B + v_C) - r(i_a + i_b + i_c) - L\frac{d(i_a + i_b + i_c)}{dt} \quad (4)$$

where $r$ and $L$ are the resistance and leakage inductance as measured from the LV side, respectively, and $N_{\mathrm{LV}}/N_{\mathrm{HV}}$ is the turns ratio. Substituting (2) and (3) into (4) gives

$$e_a + e_b + e_c = 0. \quad (5)$$

Substituting LV voltages from (1) in (5) results in

$$e_{g1g2} = -\frac{1}{3}(e_{a1g1} - e_{a2g2}) - \frac{1}{3}(e_{b1g1} - e_{b2g2}) - \frac{1}{3}(e_{c1g1} - e_{c2g2}). \quad (6)$$

Substituting the value of $e_{g1g2}$ in (1) yields

$$\begin{pmatrix} e_a \\ e_b \\ e_c \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}\begin{pmatrix} e_{a1g1} - e_{a2g2} \\ e_{b1g1} - e_{b2g2} \\ e_{c1g1} - e_{c2g2} \end{pmatrix} \quad (7)$$

The connection between LV Winding voltages and shaft voltages is communicated in (7). Post voltages rely on upon the conduction condition of the switches in VSC-1 and VSC-2. A sum of 26 = 64 separate blends of conditions of the switches is conceivable. As talked about the degree of dc-connection voltages of Vscs Vdc1: Vdc2 ought to be equivalent to 1:0.366 for better execution. Utilizing this, the voltage space vector plot comparing to extraordinary exchanging states is demonstrated in Figure 3. Out of 64 exchanging expresses, 49 states produce remarkable stage voltages, and 25 voltage steps are practical in the LV-side voltage.

The line voltages of the LV side $e_{ab}$, $e_{bc}$, and $e_{ca}$ are expressed as pole voltages using (1)

$$e_{ab} = e_a - e_b = e_{a1g1} - e_{a2g2} - e_{b1g1} + e_{b2g2}$$
$$e_{bc} = e_b - e_c = e_{b1g1} - e_{b2g2} - e_{c1g1} + e_{c2g2}$$
$$e_{ca} = e_c - e_a = e_{c1g1} - e_{c2g2} - e_{a1g1} + e_{a2g2}. \quad (8)$$

For vdc2 = 0.5vdc1, contingent upon the condition of switches, voltage waveforms of eab, ebc, and eca has seven separate steps. This is same as the quantity of steps got in the line voltage of four-level diode clipped multilevel converter. For vdc2 = 0.366vdc1, nine separate steps are seen in the line voltage waveforms, which is the same as that in four-level diode clipped converter with the capacitor voltage degree vdc1 : vdc2 : vdc3 equivalent to 0.33:0.66:0.33. This makes the proposed plan proportionate to a four-level converter.

- **PWM Strategy**

LV voltage ea takes one of the 25 qualities given by (7), built upon the condition of the switches. The switching state is chosen by the adjusting waveform and the PWM procedure utilized. Selective harmonic elimination method (SHEM), space vector modulation (SVM), or carrier based PWM (CB-PWM)

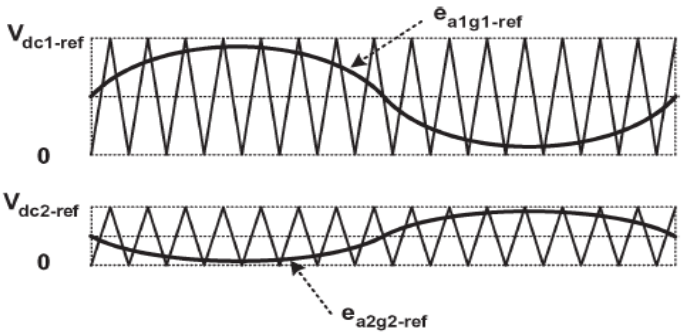


**Figure 5: Comparison of Reference and Carrier Waveforms for PS CB-PWM**

strategies are regularly utilized for high-control applications. SHEM is constrained being used in light of its abate dynamic reaction. Acknowledgment of SVM for multilevel converter requires a calculation for the distinguishing proof of part. The vicinity of vast number of divisions makes the usage complex. Thus, the utilization of stage moved (PS) CB-PWM is proposed for the proposed topology. This PWM strategy anticipates that the controller will create individual adjusting waveforms for every inverter yield ea1g1, eb1g1, ec1g1, ea2g2, eb2g2, and ec2g2. Each one tweaking waveform is contrasted with a transporter waveform with focus the exchanging condition of the comparing inverter gadgets. This is like the PS CB-PWM procedure utilized as a part of H-extension fell converters. For two H-spans every stage, the resultant waveform of air conditioning voltages is the aggregate of individual converter voltages. Accordingly, carrier waveforms are 180◦ PS from one another to drop the carrier recurrence harmonics. In any case, on account of unbalanced twin converter topology, the shift in carriers is not obliged in light of the fact that the resultant waveform is the distinction of two ac voltages. Examination of tweaking and carrier signals for stage an is indicated in Figure 4 the nonattendance of low-order harmonics affirms the operation of PWM strategy. Overwhelming music are available at the sideband of double the bearer recurrence. Despite the fact that the sidebands of bearer recurrence are likewise introduce, their extent is short of what that of double the carrier frequency.

## EQUIVALENT CIRCUIT OF THE SYSTEM

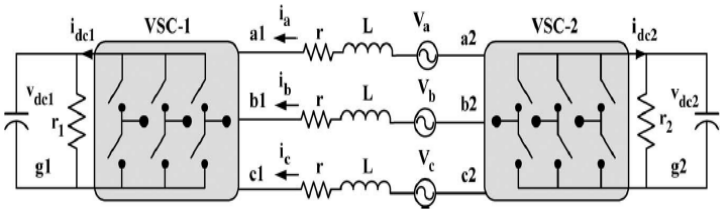


**Figure 6: Equivalent Circuit of the STATCOM**

With the end goal of investigation, a comparable circuit of the proposed STATCOM is inferred and is indicated in Figure 5. Transformer is spoken to by proportional arrangement mix of inductances, resistances, and voltage sources. To model the misfortunes in two Vscs, two resistances r1 and r2 are set in parallel to the two dc links. The administering mathematical statements of the proposed framework can be determined as

$$s\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & 0 & 0 \\ 0 & -\frac{r\omega_b}{L} & 0 \\ 0 & 0 & -\frac{r\omega_b}{L} \end{pmatrix}\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} -e_a + V_a \\ -e_b + V_b \\ -e_c + V_c \end{pmatrix} \tag{9}$$

where $L$ is defined as $\omega_b l/Z_{base}$. l, $\omega_b$, and $Z_{base}$ are the leakage inductance, base frequency, and base impedance of STATCOM. All the parameters and variables are expressed in per-unit (p.u.) system. Equation (9) is transformed into *dq*0 reference frame, The system variables in the *dq*0 frame are expressed as follows:

$$s\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & \omega \\ -\omega & -\frac{r\omega_b}{L} \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} -e_{d1} + e_{d2} + |V| \\ -e_{q1} + e_{q2} \end{pmatrix} \tag{10}$$

where $i_d$ and $i_q$ are the d- and q-axis components of LV-side currents. $e_{d1}$ and $e_{q1}$ are the voltage components of VSC-1, and $e_{d2}$ and $e_{q2}$ are the voltage components of VSC-2. Equation (10) interrelates the ac parameters of the STATCOM with those of the grid. The dependence between dc and ac parameters of STATCOM is derived using instantaneous power balance equations. The following equation gives the power balance condition between the ac and dc links of VSC-1:

$$v_{\mathrm{dc1}} i_{\mathrm{dc1}} = \frac{3}{2}(e_{d1} i_d + e_{q1} i_q) \tag{11}$$

The current flowing through the dc-link capacitor $c_1$ is related to the dc-link voltage $v_{dc1}$ as follows:

$$s v_{\mathrm{dc1}} = \omega_b C_1 \left( i_{\mathrm{dc1}} - \frac{v_{\mathrm{dc1}}}{r_1} \right) \tag{12}$$

where $C_1$ is defined as $1/(\omega_b c_1 Z_{base})$. Substituting $i_{dc1}$ from (11)

$$s v_{\mathrm{dc1}} = \omega_b C_1 \left( \frac{3}{2 v_{\mathrm{dc1}}}(e_{d1} i_d + e_{q1} i_q) - \frac{v_{\mathrm{dc1}}}{r_1} \right) \tag{13}$$

$$s v_{\mathrm{dc2}} = \omega_b C_2 \left( \frac{-3}{2 v_{\mathrm{dc2}}}(e_{d2} i_d + e_{q2} i_q) - \frac{v_{\mathrm{dc2}}}{r_2} \right) \tag{14}$$

Equations (10), (13), (14) represent the behavior of the system.

## SIMULATION RESULTS

Here Simulation is done in three separate Conditions, 1). Proposed Asymmetric Converter Based High Power STATCOM. 2). Proposed Asymmetric Converter Based High Power STATCOM with Reactive Power Control. 3) proposed Asymmetric Converter Based High Power STATCOM Applied to BLDC Motor Drive.

### Case 1: Proposed Asymmetric Converter Based High Power STATCOM

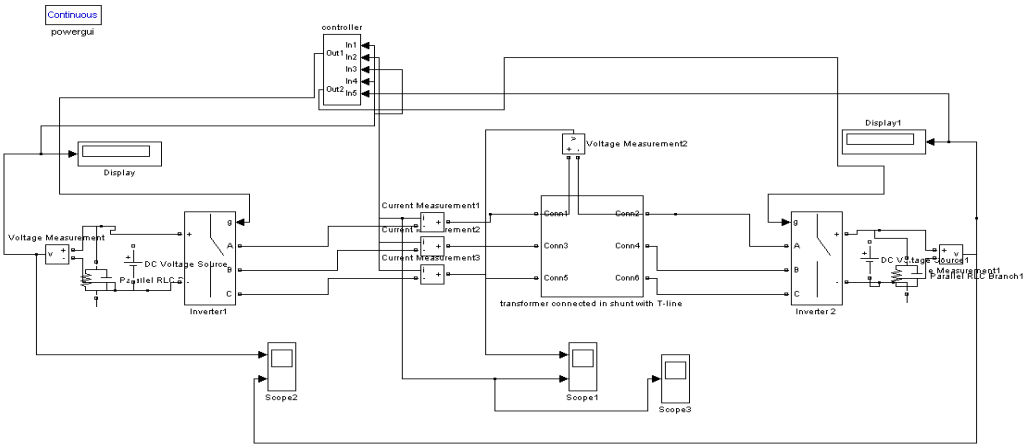


**Figure 7: Simulink Model of Asymmetric Converter of High Power STATCOM**

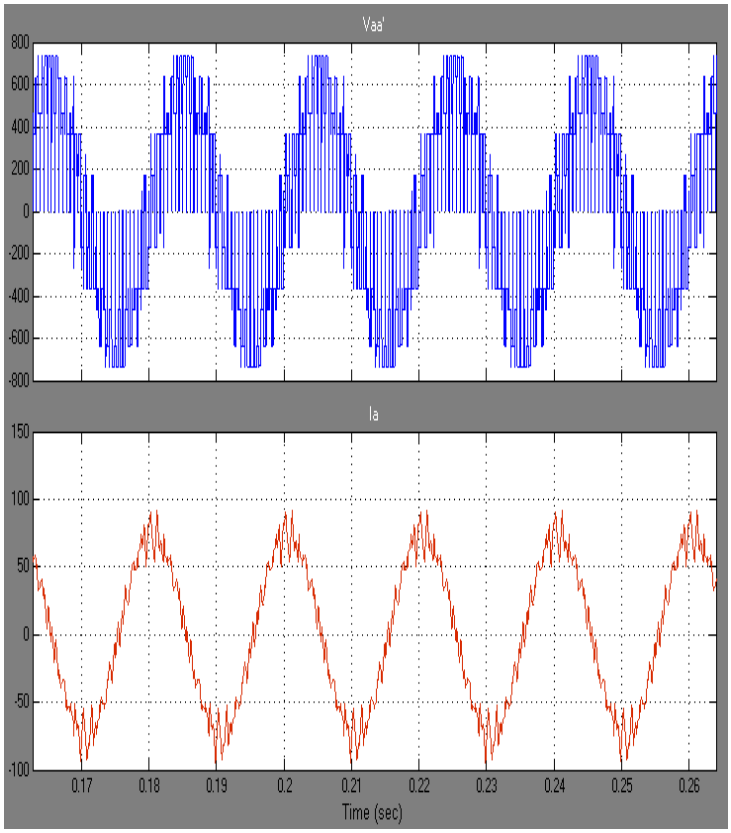


**Figure 8: High Voltage-Side (Grid) Phase-a Voltage & Low Voltage-Side Phase-a Transformer Current**

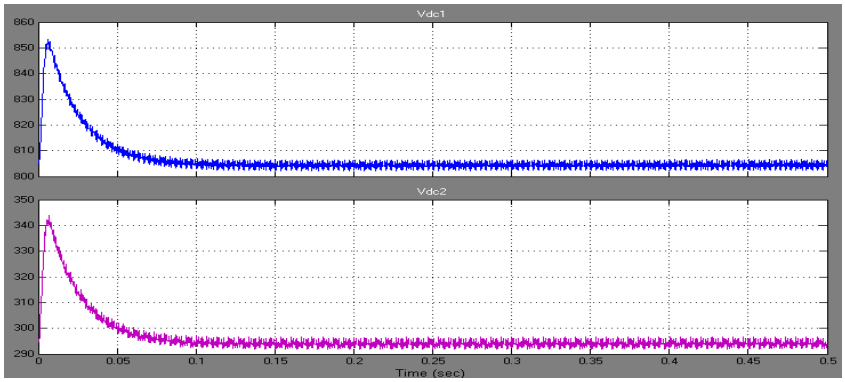


**Figure 9: Converter Side Source Voltage**

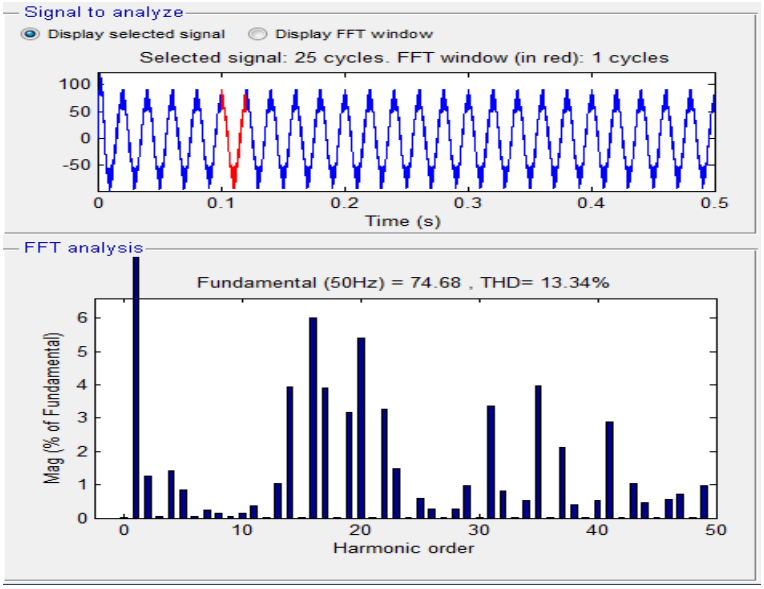


**Figure 10: FFT Analysis of Low Voltage Side Phase a Current**

Figure 10 shows the FFT Analysis of LV Side Phase a Current, we get 13.34%, with Asymmetric Converter.

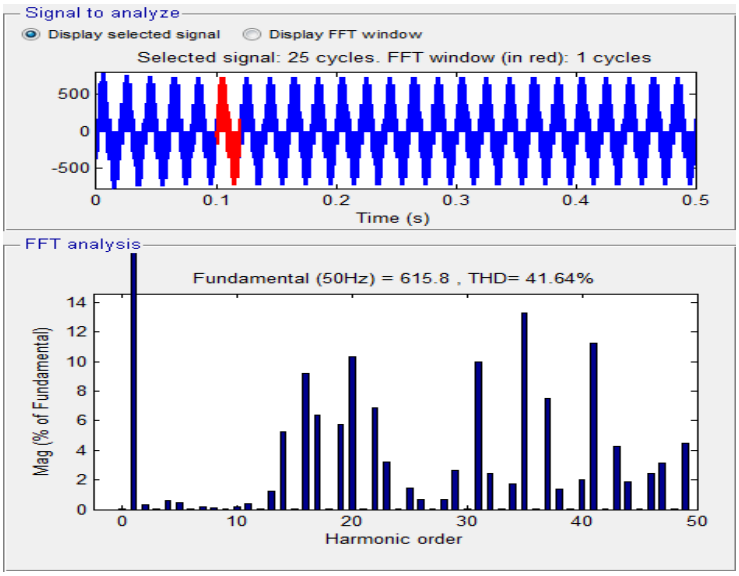


**Figure 11: FFT Analysis of Low Voltage Side**

**Case 2: Proposed Converter with High Power STATCOM with Reactive Power Control**

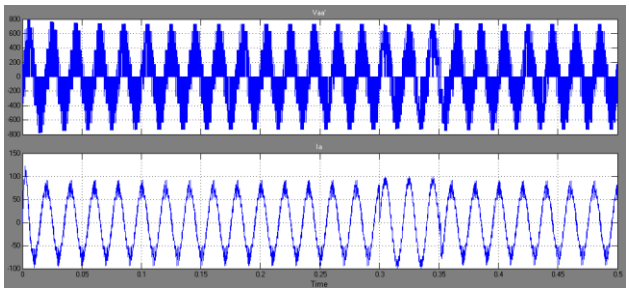

**Figure 12: High Voltage-Side (Grid) Phase-a Voltage & Low V-Side Phase-a Transformer Current**

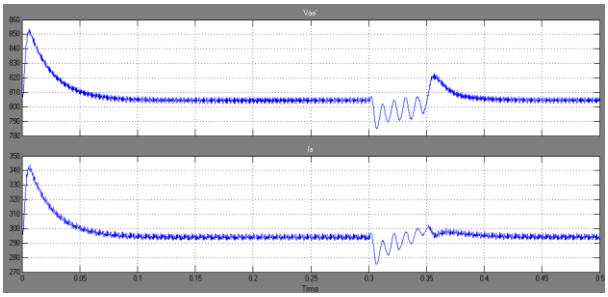

**Figure 13: Converter Side Source Voltage**

**Case 3: Proposed Asymmetric Converter Based High Power STATCOM Applied to BLDC Motor Drive**

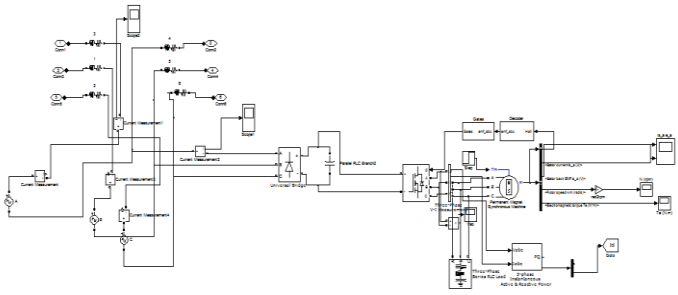

**Figure 14: Matlab/Simulink Model of Proposed Asymmetric Converter Based High Power STATCOM Connected to BLDC Drive**

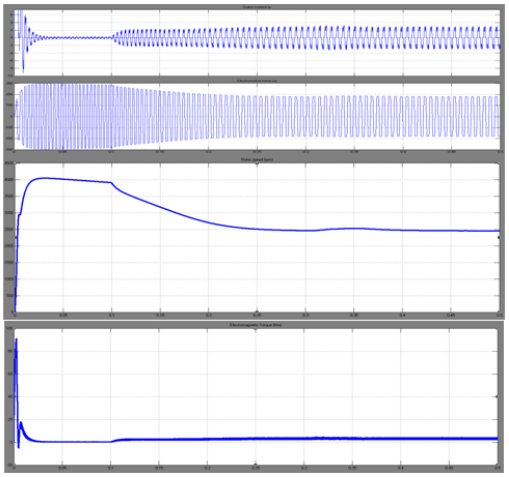

**Figure 15: Stator Current, Speed, Electromagnetic Torque**

Figure 15 shows the Stator Current, Speed, and Electromagnetic Torque of Proposed Asymmetric Converter Based High Power STATCOM Applied to BLDC Drive.

## CONCLUSIONS

Asymmetric Parallel Converter Based High-Power STATCOM Applied to BLDC Motor Drive the primary point of this idea to diminish the THD values and to check the execution of the drive. In the proposed topology, just two dc voltages must be controlled. Besides, the degree of the dc-link voltages of the two Vscs is chosen such that low distortion in current is attained. A dc-link voltage controller has been proposed to manage the dc-link voltages of the two converters by drawing essential measure of real power from the utility and by differentially appropriating them between the two converters. A Matlab/Simulink model of the framework is produced to encourage the outline of the proposed converter.

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